

**BOUNDARY SCAN DELAY CHAIN FOR CROSS-CHIP DELAY
MEASUREMENT**

Abstract

The invention relates to the delay measurement functionality of integrated
5 circuits. An object of the invention is to provide a new and improved
approach for delay measurement of an integrated circuit that is substantially
independent of vendors, technology and/or used development tools with a
minimum of implementation effort in design time and gate resources.

According to the invention, it is proposed to provide at least one boundary
10 scan cell, each having a storage layer between a scan input port (SI) and a
scan output port (SO) constructed to be used within a boundary scan chain
of an integrated circuit for boundary scan testability, to analyze each
boundary scan cell to identify a redundant state which is used to extend the
boundary scan cell by creating an additional local path (BP) between the
15 respective said scan input and scan output ports bypassing the respective
storage layer and to implement the scan cell in the integrated circuit by
creating said scan chain.